CLAIMS:

1. System on a chip (SoC) comprising
- a system bus (56),
- a high-speed functional block (51) operably linked to the system bus (56),
- a high-speed clock line (54) for applying a high-speed clock to the high-speed functional block (51),
- a peripheral bus (59),
- a low-speed functional block (52) operably linked to the peripheral bus (59),
- a circuitry (53) for generating a wait signal (PWAIT),
- a low-speed clock line (57) for applying a low-speed clock (PCLK) to the low-speed functional block (52),
- a select line (58) for feeding a select signal (PSEL) from the peripheral bus (59) to the low-speed functional block (52),
- an enable line (55) for applying a clock enable signal (PCLKEN) to the circuitry (53),
- a wait line (61) for feeding the wait signal (PWAIT) to the high-speed functional block (51),

wherein the circuitry (53) generates the wait signal (PWAIT) from the select line signal (PSEL) and the clock enable signal (PCLKEN).

2. The system of claim 1, wherein the circuitry (53) is connected to the high-speed clock line (54), the enable line (55), and the select line (58).

3. The system of claim 1, wherein the circuitry (53; 73) combines the clock enable signal (PCLKEN) with a power down signal (PDOWN_N) and the select line signal (PSEL) in order to generate the wait signal (PWAIT).

4. The system of claim 3, wherein the power down signal (PDOWN_N) is applied via a power down line (75) to the circuitry (73).

5. The system of claim 1, wherein the circuitry comprises means for generating the low-speed clock (PCLK).

6. The system in accordance with one of the claims 1 - 5, wherein the low-speed clock (PCLK) is generated from the high-speed clock and the clock-enable signal (PCLKEN).

7. The system of claim 1 or 4, wherein the circuitry is part of the low-speed functional block or wherein the circuitry is operably linked to the low-speed functional block.

8. The system of claim 1, wherein the circuitry comprises a plurality of logic gates.

9. The system of claim 1 further comprising a processor that is linked to the system bus.

10. The system of claim 1 further comprising a bridge for connecting the system bus to the peripheral bus, whereby the bridge allows an exchange of data between the high-speed functional block and the low-speed functional block.

11. The system of claim 1, wherein the system bus is a high-speed bus, preferably an AHB- or an ASB high bandwidth bus.

12. The system of claim 1, wherein the high-speed functional block is part of an AHB- or ASB domain.

13. The system of claim 1, wherein the peripheral bus is a low-speed bus, preferably a low bandwidth bus.

14. The system of claim 1, wherein the low-speed functional block is part of an APB domain.